ABSTRACT OF THE DISCLOSURE

In a potential interconnection layer, when viewed from a plane, a plurality of power supply potential regions and ground potential regions are alternately provided, with an interlayer insulation layer lying therebetween. A contact plug penetrating a second insulation layer is provided to electrically connect a source/drain (S/D) region on one side of a selected field effect transistor with a selected power supply potential region. Similarly, a contact plug penetrating the second insulation layer is provided to electrically connect a source/drain (S/D) region on the other side of another selected field effect transistor with a selected ground potential region. By employing this structure, a semiconductor device having a plurality of semiconductor circuits in which a power supply potential and a ground potential can be stabilized regardless of the cross-sectional structure of the semiconductor device is provided.